T.E. (Sem- VI) CBSGS
EXTC Engineering
VLSI Design

9/6/2015

QP Code : 5141

(3 Hours) **[Total Marks : 80**

N.B. : (1) Question **no. 1** is **compusory**.
(2) Answer **any three** questions out of **remaining** questions.
(3) Assume **suitable data** if **required**.

1. Solve any **five** :- **20**
   (a) Draw layout of 2 input CMOS NOR gate using lambda (λ) rules.
   (b) Implement Master Slave D Flip Flop using C^2MOS logic style.
   (c) Explain various sources of power dissipation in CMOS Inverter.
   (d) Implement NOR based 2:4 decoder.
   (e) State various short channel effects and explain one of them.
   (f) Draw static CMOS NAND and NOR gates. Size all transistors in NAND and NOR gate to provide worst case equal rise and fall delay for both gates. Assume mobility of electron is two times higer than that of holes. Magnitude of threshold voltage for all transistor is same.

2. (a) Draw six transistor CMOS SRAM cell. Describe various constraints that should be imposed on the devices for guaranteeing safe read and write operation. Derive the equation that would help to size the transistors and also based on derived equations, discuss qualitatively relative sizing of transisters in the cell. **10**

   (b) Implement $Y = \overline{AB + C(D+E)}$ using **10**
   (i) Static CMOS logic.
   (ii) Dynamic logic with pull up network.
   (iii) Dynamic logic with pull down network.
   (iv) Pesudo NMOS logic.

3. (a) With the help of neat cross sections and appropriate masks, give the process flow of N-well CMOS technology. **10**

   (b) For CMOS Inverter with following parameters. **10**

$$V_{TO,n} = 0.6\ V \qquad \mu_n C_{ox} = 60\mu A/V^2, \left(\frac{W}{L}\right)_n = 8$$

$$V_{TO,p} = -0.7\ V \qquad \mu_p C_{ox} = 20\mu A/V^2, \left(\frac{W}{L}\right)_p = 12$$

Calculate noise margins and the switching threshold of the inverter. The power supply voltage $V_{DD} = 3.3$ V.

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4. (a) Design clocked CMOS JK latch to implement the truth table shown below. **10**

Clk	J	K	$Q_{n+!}$
1	0	0	Q_n
1	0	1	0
1	1	0	1
1	1	1	$\overline{Q}_n$ (toggle)

(b) Explain 4 × 4 bit array muiltiplier with the help of necessary hardware for the generation and addition of partial product. **10**

5. (a) In two input CMOS NAND gate , $\mu_n C_{ox} = 20\mu A/V^2$, $\mu_n C_{ox} = 10\mu A/V^2$, and all PMOS have $\left(\frac{W}{L}\right)_n = 20$, $V_{TO,n} = 1$ V and $V_{TO,p} = -1$ V. If one of the input is held permenantly at V_{DD} and other is switched from zero volts to V_{DD} with zero rise time for a duration grater than fall delay of NAND gate and then switched back to zero volts with zero fall time, then calculate t_{pHL} and t_{pLH}. Asume V_{DD} = 5V and total load capacitance which is independent of MOSFET sizes is equal to 2PF. **10**

(b) With the help of suitable diagrams explain how clock is generated and stabilized in VLSI chip. **5**

(c) Explain with help of neat diagrams importance of power distribution network in VLSI chip. **5**

6. Write short notes on any **four** :- **20**
   (a) **Flash memory**
   b) **Carry look ahead adder**
   (c) ESD protection circuit
   (d) Barrel Shifter
   (e) Interconnect scalling.

T.E-Sem VI (CBGS) (EXTC) 3/6/15

Operating Systems

Q.P. Code : 5140

(3 Hours) **[Total Marks : 80**

N.B. : (1) Question No. **1** is **compulsory**.
(2) Answer any **three** out of the remaining questions.
(3) Assume suitable **data** if **necessary**
(4) Assumptions made should be **clearly** stated.

1. (a) What is operating system? Explain the different functions of OS. **5**
   (b) What is system call? Explain any five system calls. **5**
   (c) Describe the structure of an I -Node in UNIX. **5**
   (d) What are the different characteristics of real time operating systems? **5**

2. (a) What is deadlock? What are the necessary and sufficient conditions to occur deadlock? Explain deadlock avoidance and Prevention. **10**
   (b) Describe process management in Linux. **10**

3. (a) Explain various page replacement algorithms with example. **10**
   (b) Explain the working of EDF and RMA real time scheduling algorithms. **10**

4. (a) Explain RAID with Different levels. **10**
   (b) Consider a following set of processes, with length of CPU bursts given in milliseconds as follows: **10**

Process	**Burst Time**	**Arrival Time**	**priority**
P1	8	0	3
P2	1	1	1
P3	3	2	2
P4	2	3	3
P5	6	4	4

(i) Draw the Gantt Charts for FCFS, SJF, Preemptive priority and RR (Quantum = 2)
(ii) What is the turnaround time of each process for above algorithms?
(iii) What is the waiting time of each process for each of the above algorithms
(iv) Which algorithms results in minimum average waiting time.

5. (a) Explain the linked and indexed methods for allocating a disk space to a file. 10

(b) How is a directory system useful in file organization? Explain single level, Two level and Hierarchical directory system. 10

6. Write a note on (any **two**) : 20

(a) Cyclic Schedulers

(b) Linux file System

(c) Unix Security measures

TE (sem VI) (CBGS) Electronics & Telecom
Television Engineering 28/5/2015

QP Code : 5136

(3 Hours) **[Total Marks : 80**

N. B. : (1) Question No. **1** is **compulsory**.
(2) Attempt **any three** out of remaining five questions, each carrying 20 marks (Q.2 to Q.6) is from all the modules.
(3) Assume any **suitable data** wherever required but **justify** the same.
(4) Illustrate answer with sketches and examples wherever required.
(5) Answer to questions should be grouped and written together.

1. (a) An odd number of lines are chosen in television system for scanning. Justify **5**
(b) What is compatibility in TV transmission? What are the requirements to be met to make the colour system fully compatible? **5**
(c) Compare Plasma, LED and LCD displays. **5**
(d) Explain in brief Direct-to-home TV (DTH). **5**

2. (a) Explain with the help of suitable sketch, how is video signal developed in a vidicon camera tube? How is different from other camera tubes and what are its special applications? **10**
(b) Draw the block diagram of PAL TV receiver and explain the working and functions of each block. **10**

3. (a) What is the difference between component video and composite video? Give the main features of CCIR Rec.601 for digital video standards **10**
(b) Describe new TV standards and compatibility adopted for HDTV. Explain MUSE system and its advantages. **10**

4. (a) Sketch composite video signal waveform for at least three successive line and indicate: **5**
(i) Extreme white level
(ii) Blanking level
(iii) Pedestal height
(iv) Sync. pulse level

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(b) Only (R-Y) and (B-Y) colour difference signals along with luminance signal is chosen for transmission. Justify the statement. Also explain why it is necessary to weight down the chrominance signal. **10**

(c) What are the technical advantages of using digital technology in television systems? **5**

5. (a) What is the need of MAC encoding? Explain the general format of MAC signals for transmitting colour TV signals. **10**

(b) Explain the following terms of Digital video. **10**

(i) Digitization

(ii) Viewing distance and angle

(iii) Aspect ratio

6. (a) Explain Interlace Scanning? Calculate the percentage of interlace error when the second field is delayed by 16 microseconds. Retrace time may be assumed to be negligible. **10**

(b) Write a note on Wide Dimension High Definition Television and its standards. **10**

TE - SEM VI (CBSGS) - EXTC

May 2015

CCTN

QP Code : 5133

(3 Hours) **[Total Marks : 80**

N. B. : (1) Question No. **1** is **compulsory**.
(2) Attempt any **three** questions from remaining **five** questions.
(3) **All** questions carry **equal** marks.

1. (a) List the Networking components and map all networking components with OSI layer. **5**
   (b) What are the components in ATM? Explain it in brief. **5**
   (c) What do you mean by multiple access? Compare between CSMA/CD & CSMA/CA. **5**
   (d) What do you mean by decentralized peer to peer file sharing? How it is different from centralized system? **5**

2. (a) Identify from IPV4 header **5**
      (i) Which feild gives no. of hops count
      (ii) What is the minimum and maximum length of HLEN
      (iii) What are the differenciate services explain TOS bits.
      (iv) Which feilds are releated to fragmentation process.
      (v) How to calculate total length. Give the functional difference between IPV4 & IPV6.
   (b) Which protocol send the error messages back to the source? Explain th query messages of ICMP. **15**

3. (a) Explain the classful addresses of IPV4 with net-id and host-id. **10**
   (b) An ISP are granted a block of addressess starting with 120.60.4.0/20. The ISP wants to distribute these blocks to 100 organizations with each organization receiving 8 address only. Design subblocks and give the slash notation for each subblock. find out how many addresses are still available after these allocations. **10**

4. (a) Classify routing protocol? Explain in brief the concept of link state and distance vector algorithms with examples. **10**
   (b) What is the role of domain name server? Explain working of DNS server with different records. **10**

5. (a) Explain in brief DSL and HFC. **10**
   (b) Draw and explain the architecture of IEEE 802.11. **10**

6. (a) What do you mean by flow control compare flow control techniques. **10**
   (b) Explain in detail the different transmission media. **10**

JP-Con. : 10241-15.

T.E. Extc Sem VI (CBGS) 18/5/15

DTSP

QP Code : 5131

(3 Hours) **[Total Marks : 80**

N.B.: (1) Question **No.1** is **compulsory.**
(2) Solve any **three** questions from remaining questions.
(3) In all **four** questions to be attempted.
(4) **Figures** to the **right** indicate **full** marks.

1. (a) Sketch the frequency response and identify the following filters based on their pass band **20**

(i) $h[n] = \left\{1, -\frac{1}{2}\right\}$

(ii) $H[z] = \frac{z^{-1} - a}{1 - az^{-1}}$

(b) Justify DFT as a linear transformation.

(c) Explain the frequency warping in Bilinear transformation.

(d) What is multi rate DSP ? Where it is required ?

2. (a) An analog filter has transfer function **8**

$$H(s) = \frac{s + 0.1}{(s + 0.1)^2 + 16}$$

Determine the transfer function of digital filter using bilinear transformation. The digital filter should have specification $\omega_r = \frac{\pi}{2}$

(b) Explain the effects of coefficient quantization in FIR filters. **8**

(c) The first five points of eight point DFT of real valued sequence are **4**
{ 0.25, 0.125-j0.3018, 0, 0.125-j0.0518, 0 }.
Determine the remaining three points.

3. (a) $x[n] = \begin{cases} 1, & 0 \le n \le 3 \\ 0, & 4 \le n \le 7 \end{cases}$ **10**

(i) Find DFT X [k]

(ii) Using the result obtained in (i) find the DFT of the following sequences.

$$x_1[n] = \begin{cases} 1, & n = 0 \\ 0, & 1 \le n \le 4 \\ 1, & 5 \le n \le 7 \end{cases} \quad \text{and} \quad x_2[n] = \begin{cases} 0, & 0 \le n \le 1 \\ 1, & 2 \le n \le 5 \\ 1, & 6 \le n \le 7 \end{cases}$$

(b) Implement a two stage decimator for the following specifications: Sampling rate of the input signal= 20,000 Hz **10**

M = 100

Pass band = 0 to 40 Hz , Pass band ripple = 0.01,

Transition band = 40 to 50 Hz, Stop band ripple = 0.002

4. (a) By means of FFT-IFFT technique compute the linear convolution of x [n] = {2,1,2,1} and h [n] = {1,2,3,4} **8**

(b) Consider the following specifications for a low pass filter **8**

$0.99 \le |H(e^{j\omega})| \le 1.01 \quad 0 \le \omega \le 0.3\pi$ and

$|H(e^{j\omega})| \le 0.01 \quad 0.5\pi \le |\omega| \le \pi$

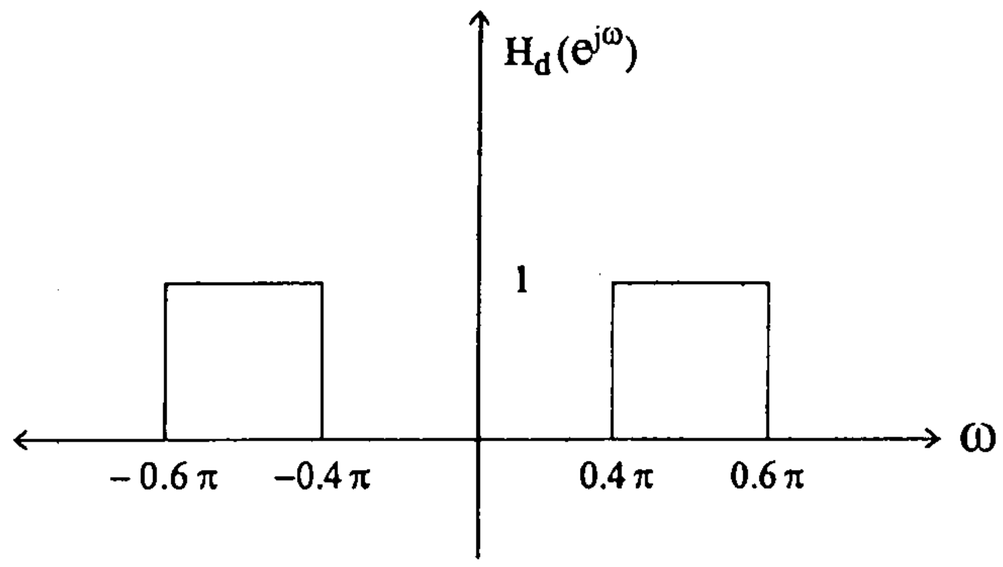
Design a linear phase FIR filter to meet these specifications using the window design method.

(c) Identify whether the following system is minimum phase, maximum phase, mixed phase. **4**

(i) $H_1(z) = 6 + z^{-1} + z^{-2}$

(ii) $H_2(z) = 1 - z^{-1} - 6z^{-2}$

5. (a) Design digital FIR filter for following specification. **10**



Use hamming window and assume M = 7.

(b) Design digital low pass IIR Butterworth filter for the following specifications: 10

pass band ripple: $\leq$ dB

pass band edge: 4 kHz

stop band attenuation: $\geq$ 40dB

stop band edge : 6 kHz

Sample rate : 24 kHz

Use bilinear transformation

6. (a) Write a short note on 12

(i) Dual tone Multi-frequency Signal Detection.

(ii) Different methods for digital signal Synthesis.

(b) The transfer function of digital causal system is given as follows : 8

$$H(z) = \frac{1 - z^{-1}}{1 - 0.2z^{-1} - 0.15z^{-2}}$$

Draw cascade form, parallel form realization.

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(79) T.E. (EXTC) - VI 12/5/2015

Digital Communication

Q.P. Code : 5127

(3 Hours) **[Total Marks : 80**

N.B: (1) Question No.**1** is **compulsory.**
(2) Attempt any three out of remaining five questions.
(3) **Figures** to the **right** indicate marks.

1. Attempt any four :
   (a) Consider an extremely noisy channel having a bandwidth of 1 kHz. What could be the channel capacity? **5**
   (b) Consider a binary data sequence 1111101111. Draw the waveforms for the given binary data sequence, using Bipolar AMI RZ and Manchester. **5**
   (c) State two criteria which a spread-spectrum communication system must satisfy. Justify that the spread-spectrum signals are transparent to the interfering signals, and vice-versa. **5**
   (d) What is the significance of Euclidian distance? **5**
   (e) Define code rate, hamming distance and Hamming weight in the context of linear block code .Also explain linearity property and cyclic property of linear codes. **5**

2. (a) Consider an alphabet of a discrete memory less source having five different source symbols with their respective probabilities as 0.1, 0.2, 0.4, 0.1, and 0.2. **10**
   (i) Create a Huffman Tree for Huffman source coding technique.
   (ii) Tabulate the codeword and length of codewords for each source symbol.
   (iii) Determine the average codeword length of the specified discrete memoryless source.
   (iv) Comment on the results obtained

   (b) A convolution code is described by generator sequence $G_1=(1, 1, 1)$ and $G_2=(1,0,1)$ **10**
   (i) Draw the encoder for this code.
   (ii) Draw the state transition diagram for this code.
   (iii) Draw the trellis diagram for this code.

3. (a) Explain how matched filter and Correlator are two ways of synthesizing optimum filter. What is matched filter? 10

(b) For a Quadrature Phase Shift Keying (QPSK), Explain the modulator, synchronous demodulator, Bandwidth and advantages. 10

4 (a) What is coherent demodulator? Describe coherent detection method of binary FSK signals. Also draw power spectra for BFSK modulated signal. 10

(b) In a digital communication system, the bit rate of a bipolar NRZ data sequence is 1 Mbps and carrier frequency of transmission is 100MHz. Determine the symbol rate of transmission and the bandwidth requirement of the communications channel for 10

(i) 8-ary PSK system

(ii) 16-ary PSK system.

5. (a) Parity check matrix for (7, 3) code is given below 10

$$H = \begin{bmatrix} 0111000 \\ 1010100 \\ 1100010 \\ 1110001 \end{bmatrix}$$

Construct syndrome table for signal bit error patterns. Using syndromes, find error pattern and codeword for each of the following received vectors

$r_1 = 0011101$, $r_2 = 1101110$.

(b) A (7. 4) cyclic code is described by a generator polynomial 10

$g(x) = 1 + x + x^3$

(i) Find the codeword using polynomial division method for m = 1010

(ii) Design an encoder for systematic code generation and explain its working.

(iii) Design a syndrome generator and explain how received message is corrected?

6 Attempt the following (any two) : 20

(a) What do you mean by an eye diagram? What is its purpose? Mention the four parameters observed from the eye pattern. Explain with the help of suitable illustration.

(b) Explain with the help of block diagrams and waveforms, the following techniques of spread spectrum communication.

(a) Direct sequence (b) Frequency hopping.

(c) Viterbi decoding algorithm for convolution codes.
